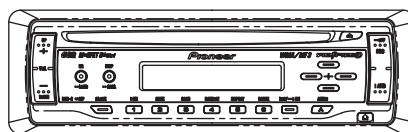


# Service Manual



DEH-2800MP/XN/UC

ORDER NO.  
**CRT3554**

HIGH POWER CD/MP3/WMA PLAYER WITH FM/AM TUNER

# DEH-2800MP /XN/UC

## DEH-2850MP /XN/ES

This service manual should be used together with the following manual(s):

Model No.	Order No.	Mech. Module	Remarks
CX-3164	CRT3583	S10.5COMP1	CD Mech. Module : Circuit Descriptions, Mech. Descriptions, Disassembly

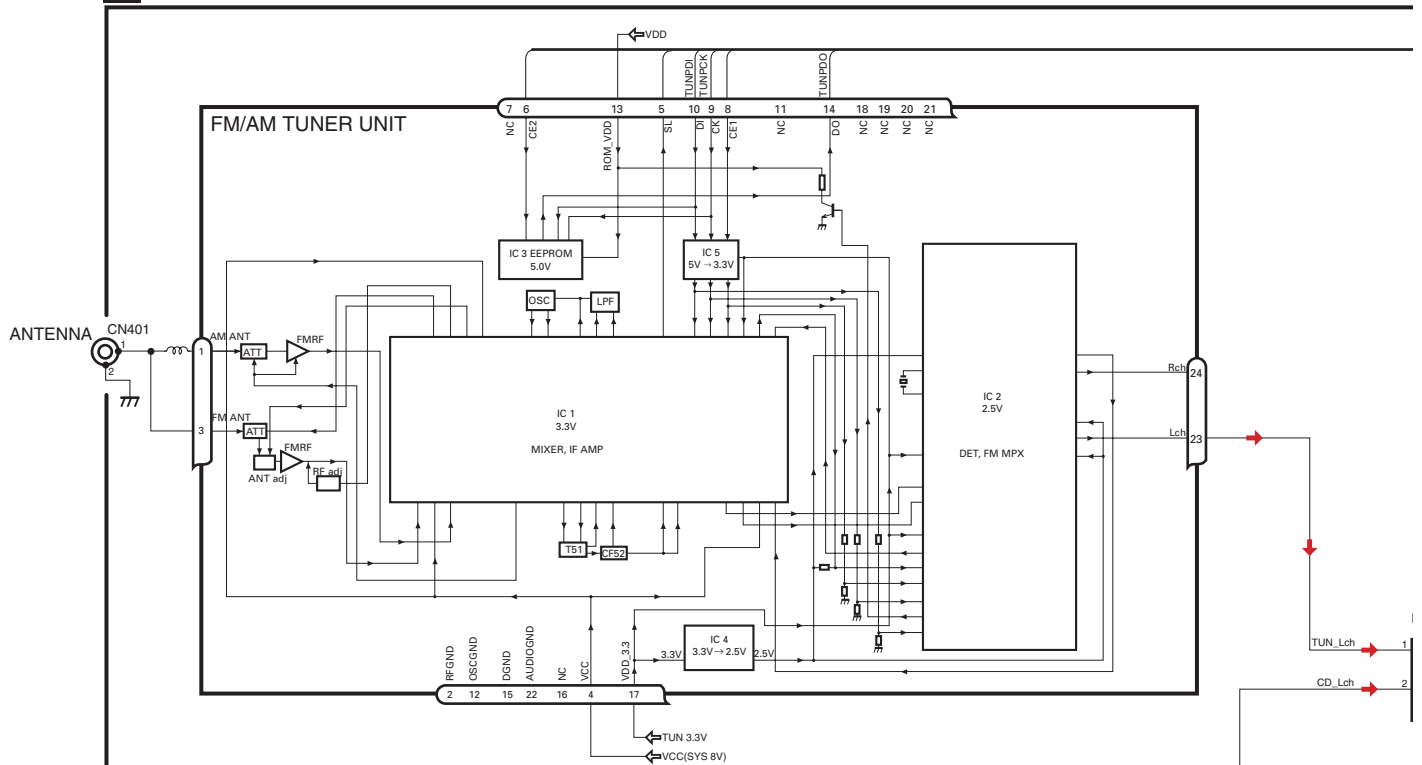


For details, refer to "Important Check Points for Good Servicing".

# 3. BLOCK DIAGRAM AND SCHEMATIC DIAGRAM

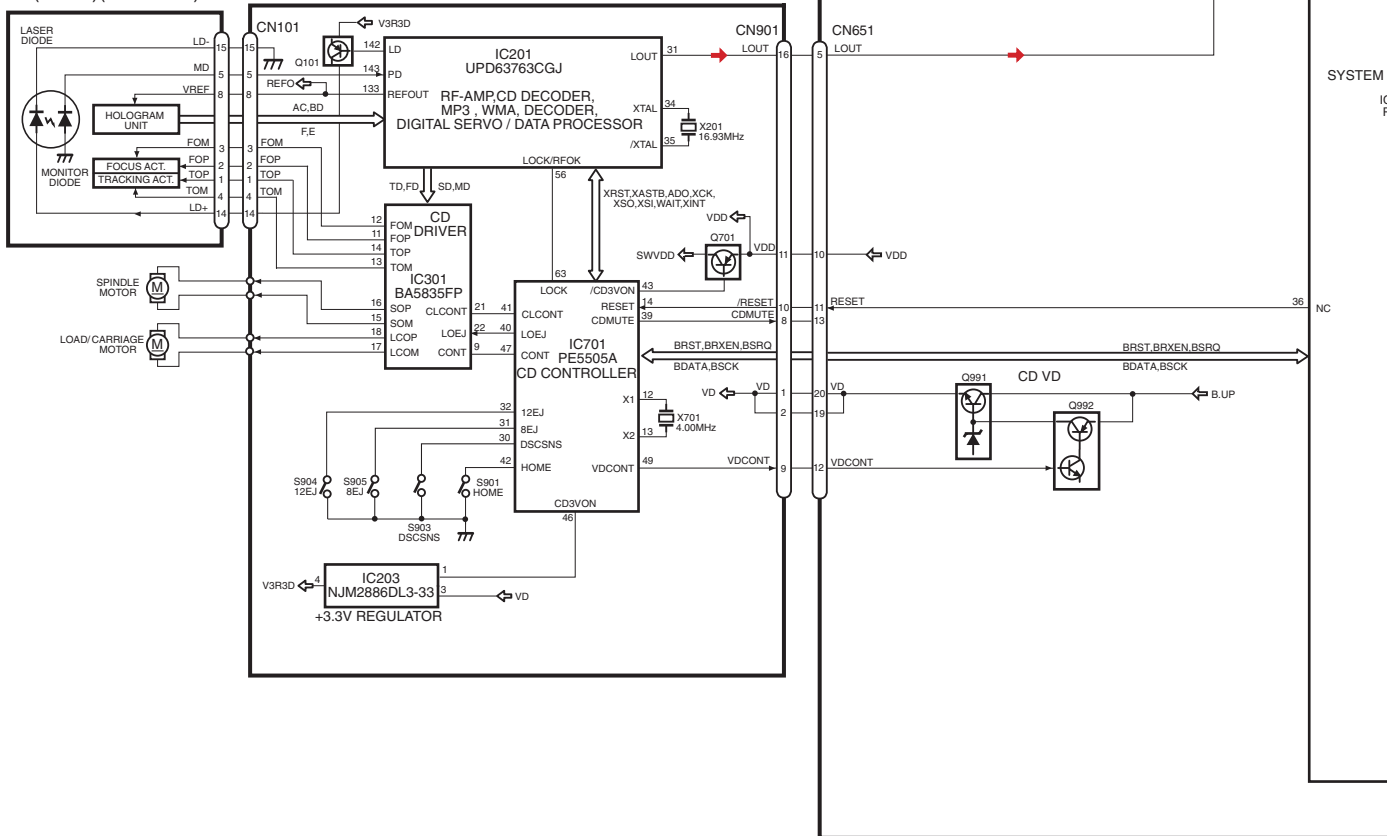
## 3.1 BLOCK DIAGRAM

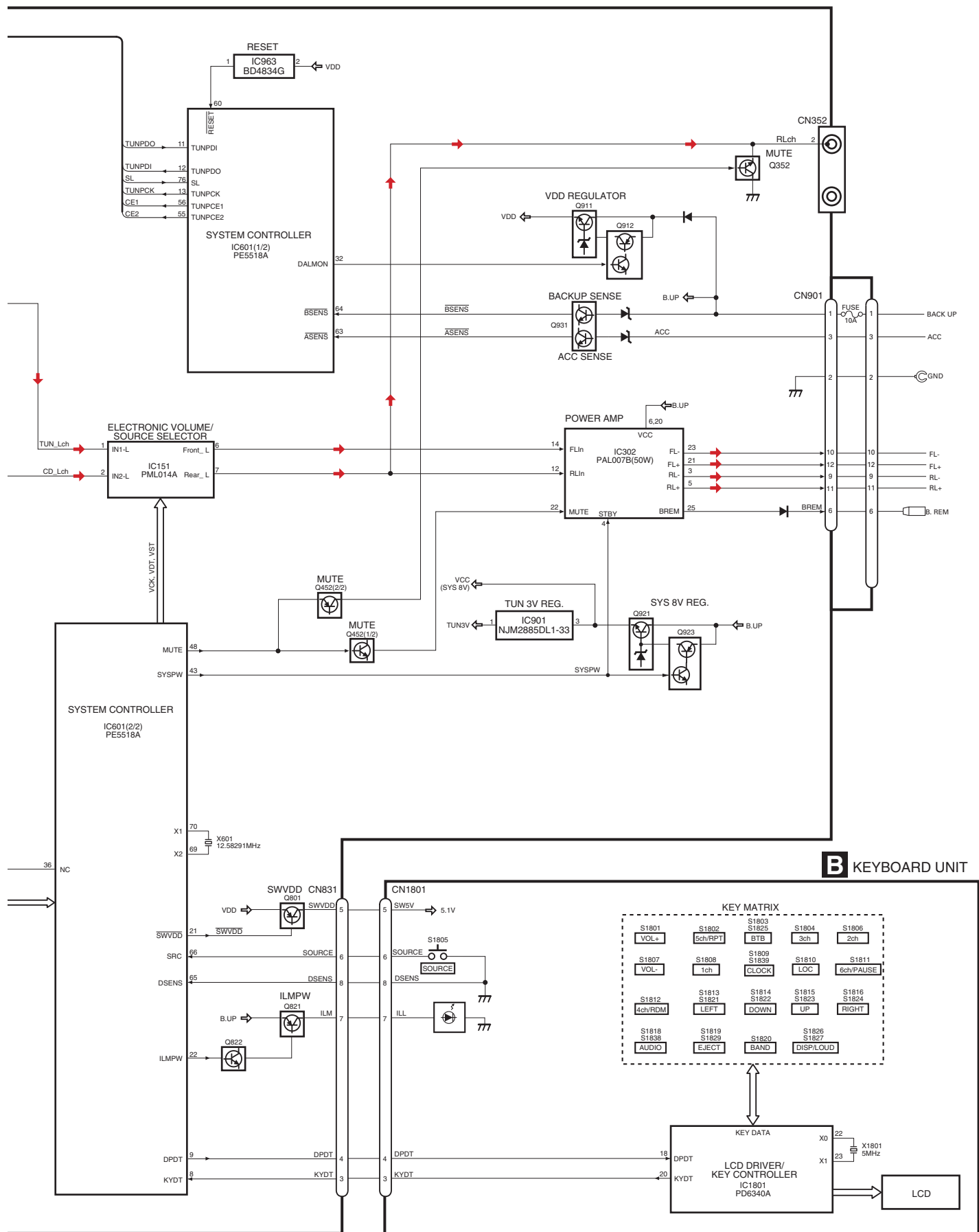
### A TUNER AMP UNIT



### PICKUP UNIT (P10.5)(SERVICE)

### C CD CORE UNIT(S10.5COMP1)

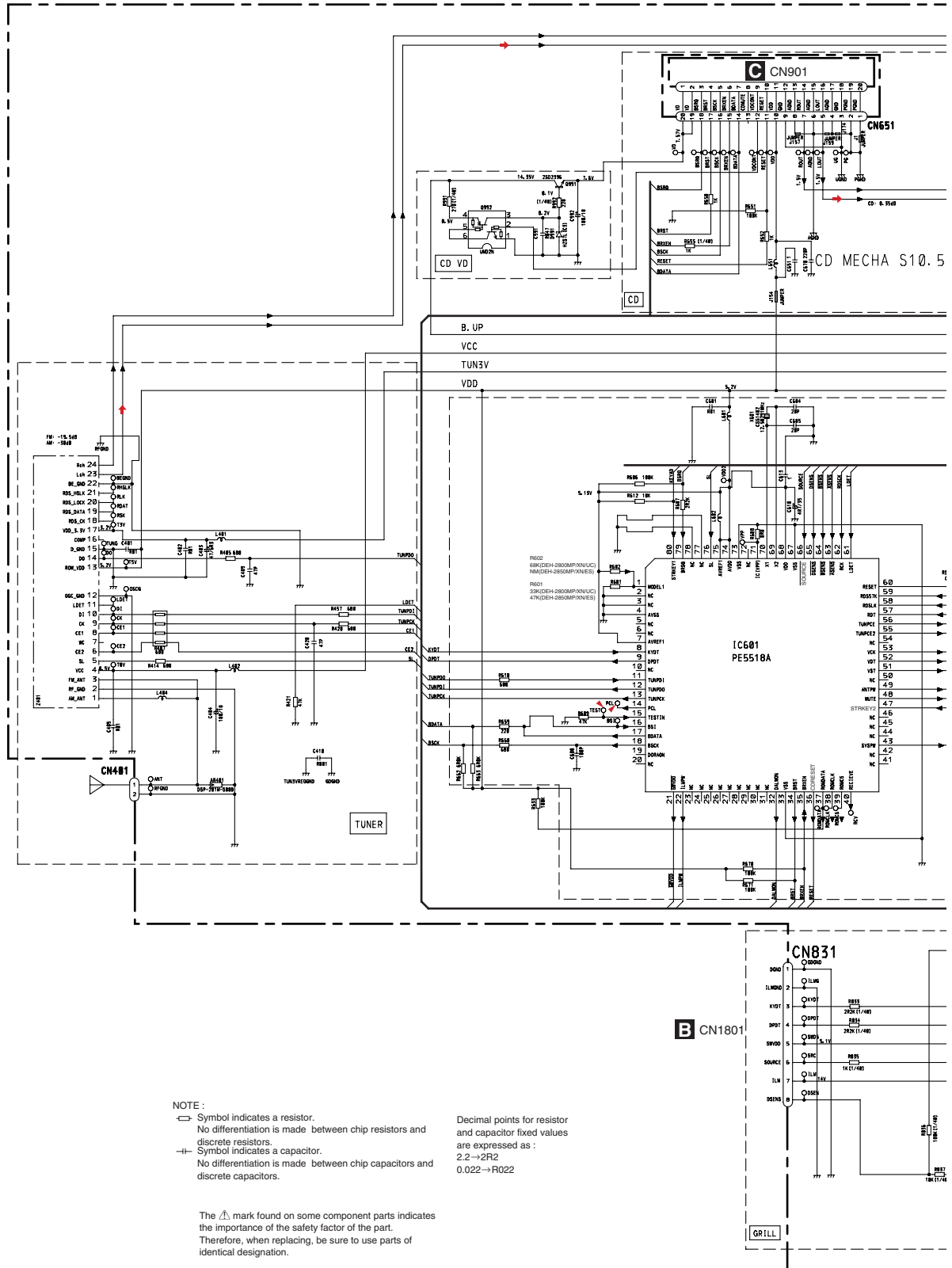
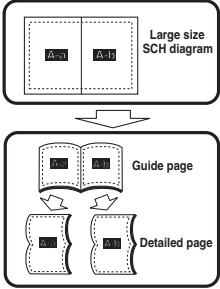




## 3.2 OVERALL CONNECTION DIAGRAM(GUIDE PAGE)

Note: When ordering service parts, be sure to refer to "EXPLODED VIEWS AND PARTS LIST" or "ELECTRICAL PARTS LIST".

A-a



A

**A** TUNER AMP UNIT

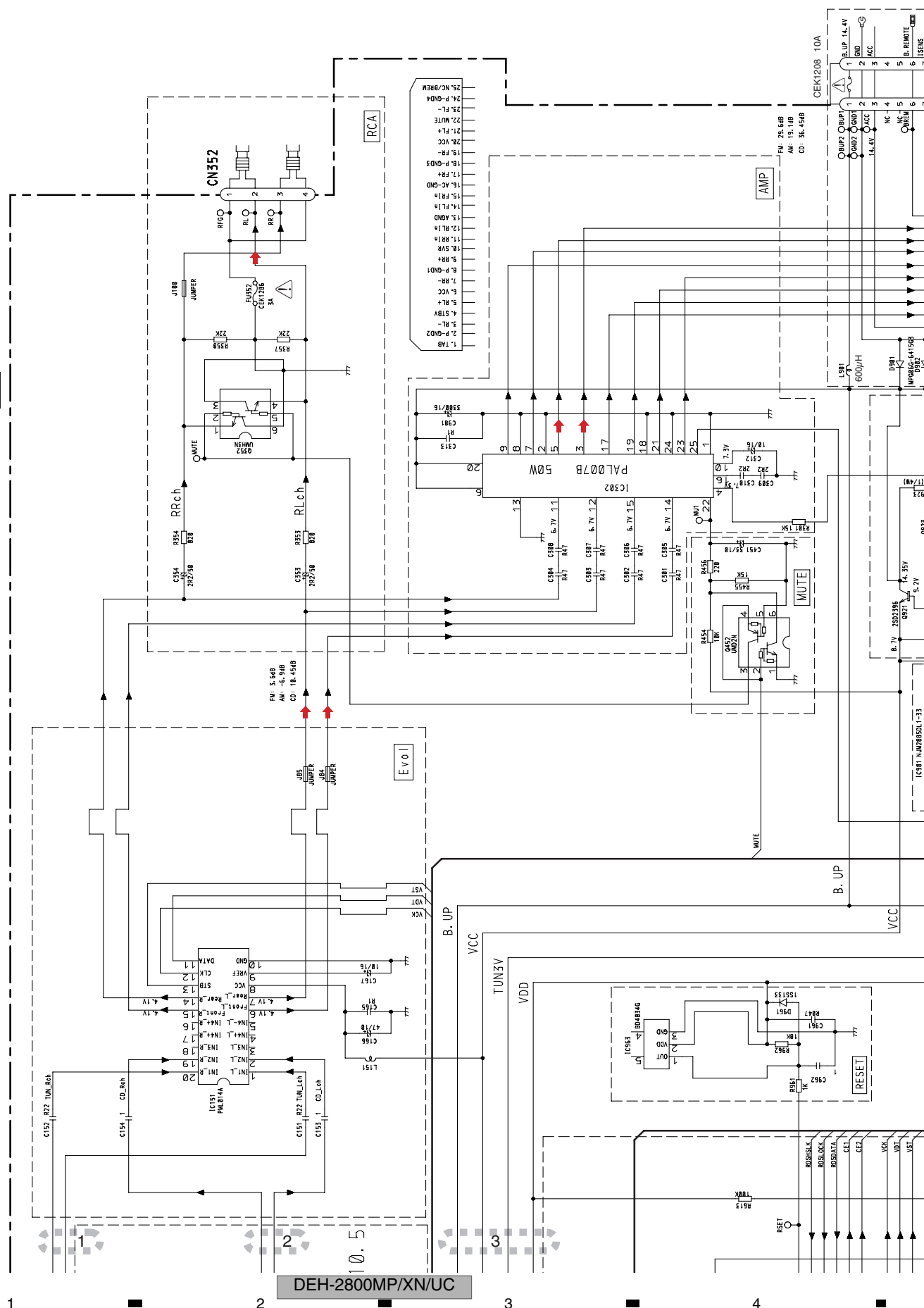


A-a A-b

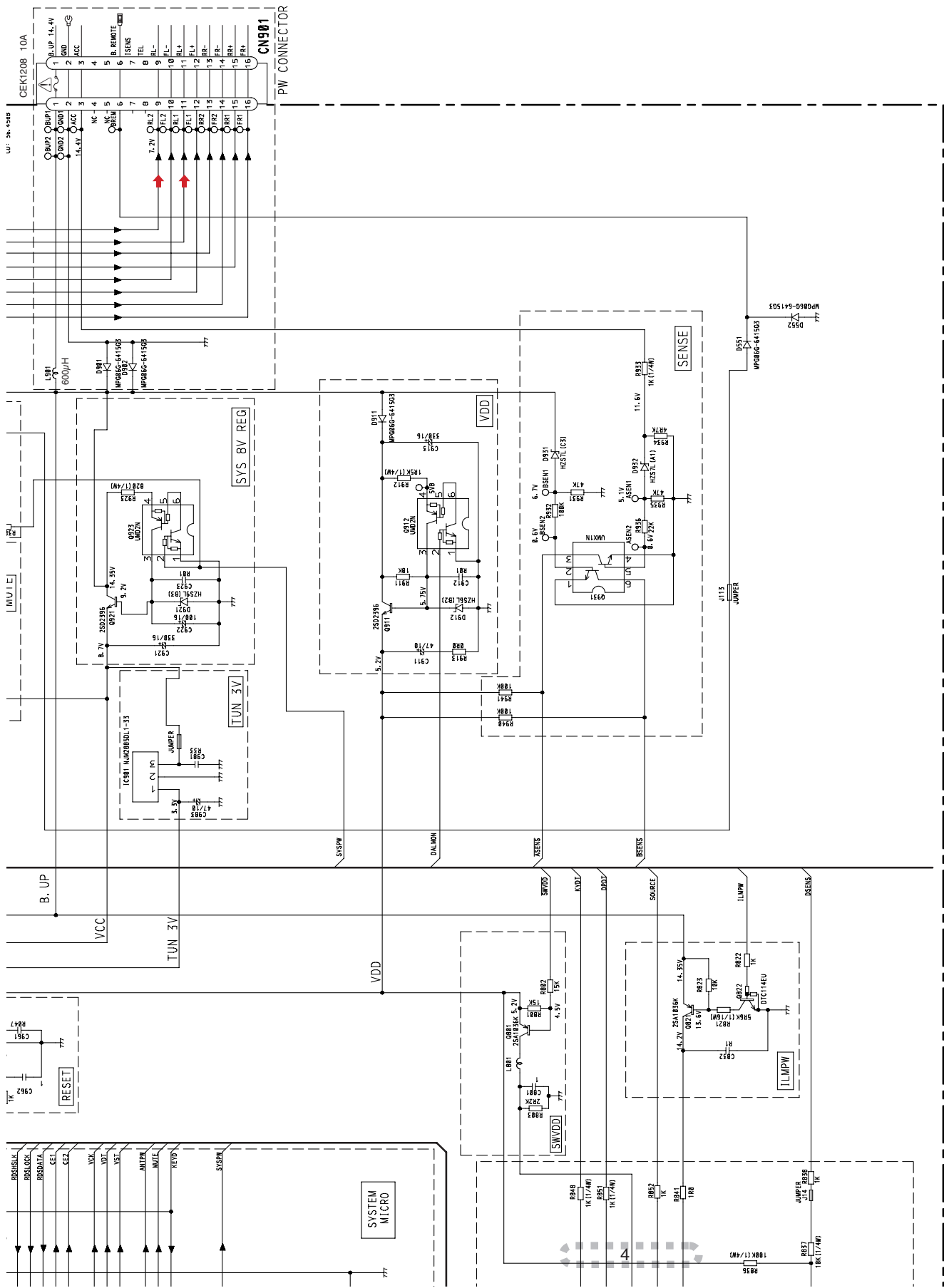




A-a	A-b
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**A-b**



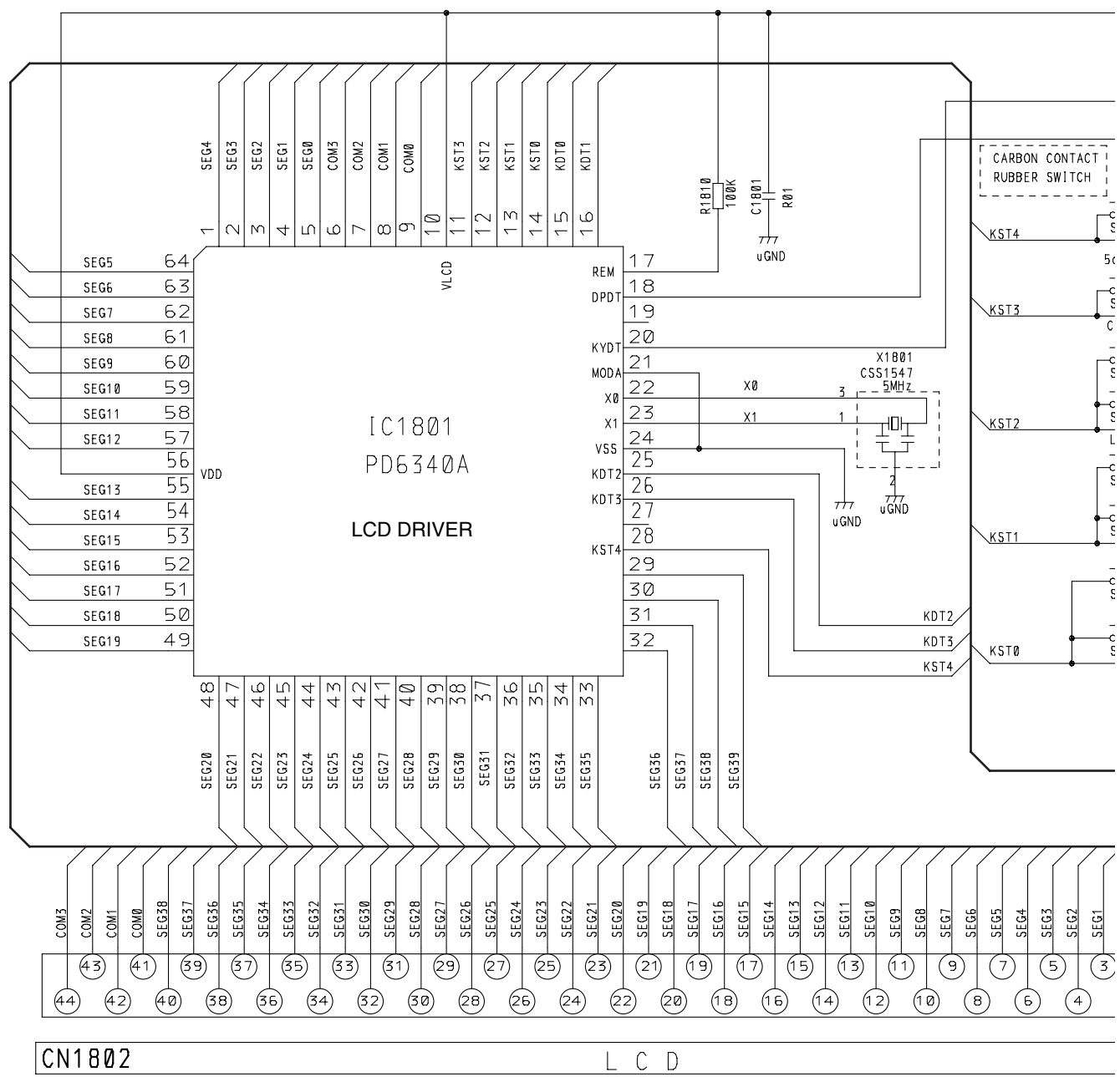


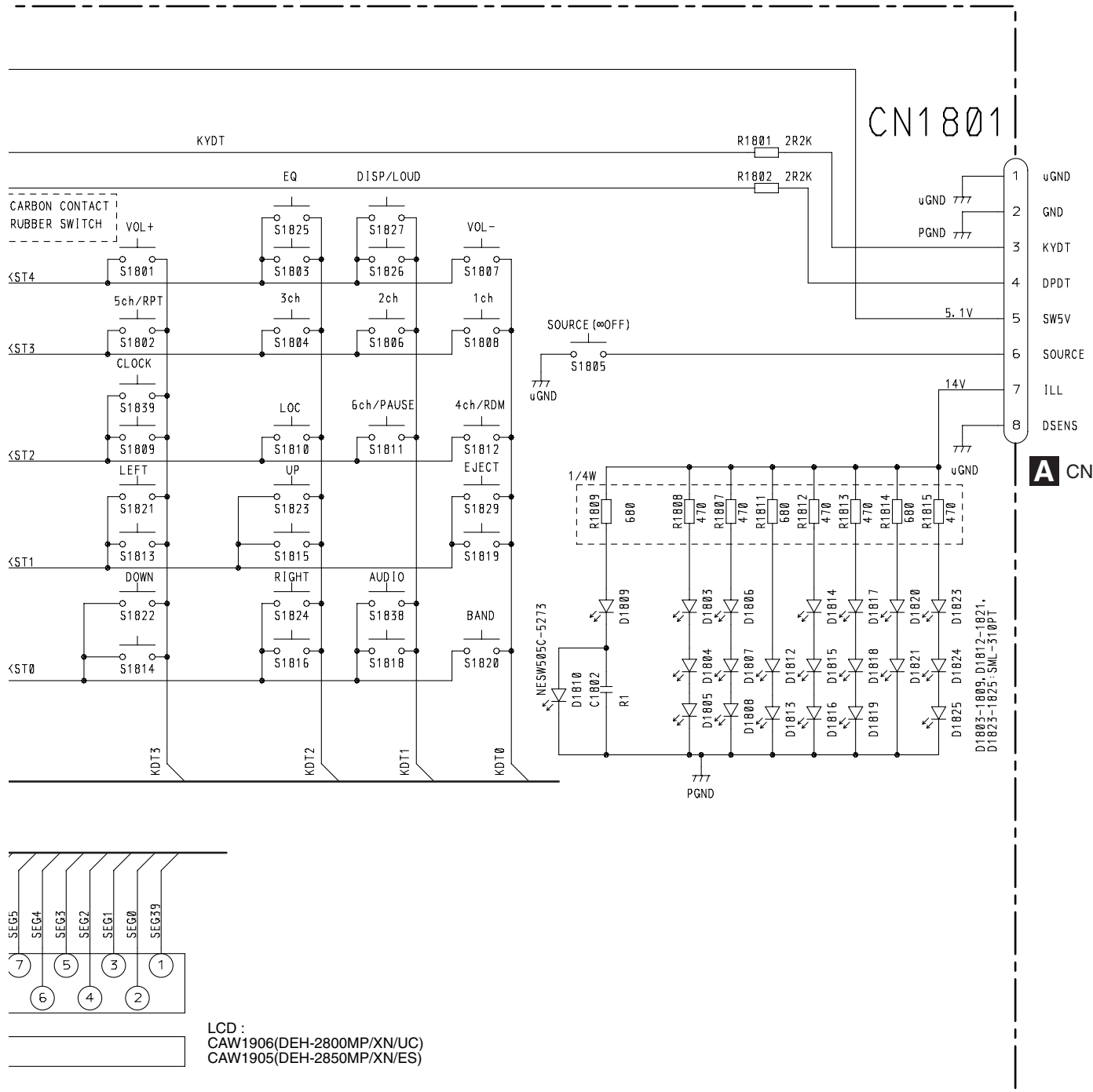
A-a A-b

A-b

3.3 KEYBOARD UNIT

B KEYBOARD UNIT



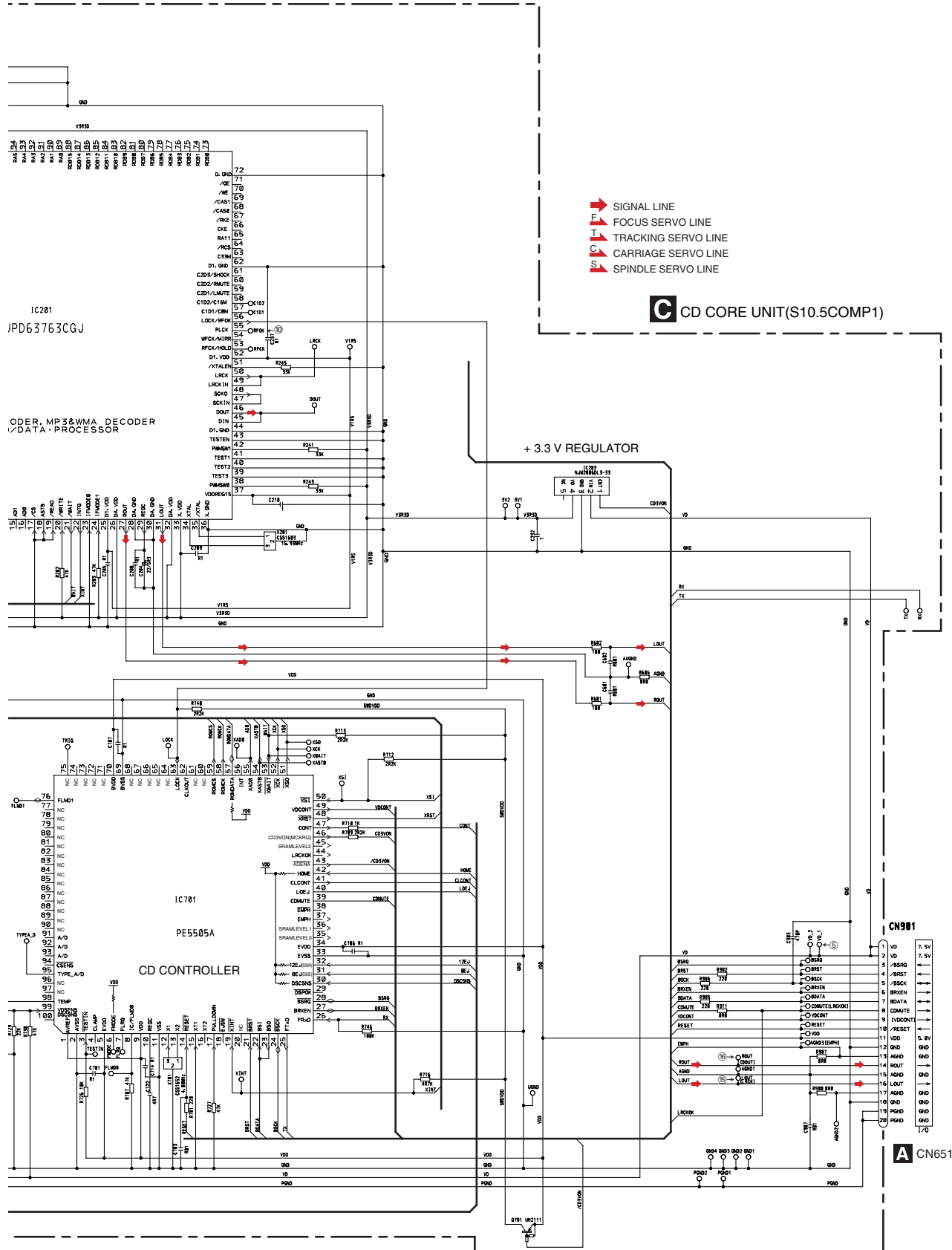


**C-a**



NOTE1) GND ... CD LSI, RFAMP, CPU  
PGND ... Actuator, Motor Driver  
AGND ... Audio  
These GND's are not connected to each other on PCB.  
PGND is connected to a floating mechanism part by a screw.

C-b



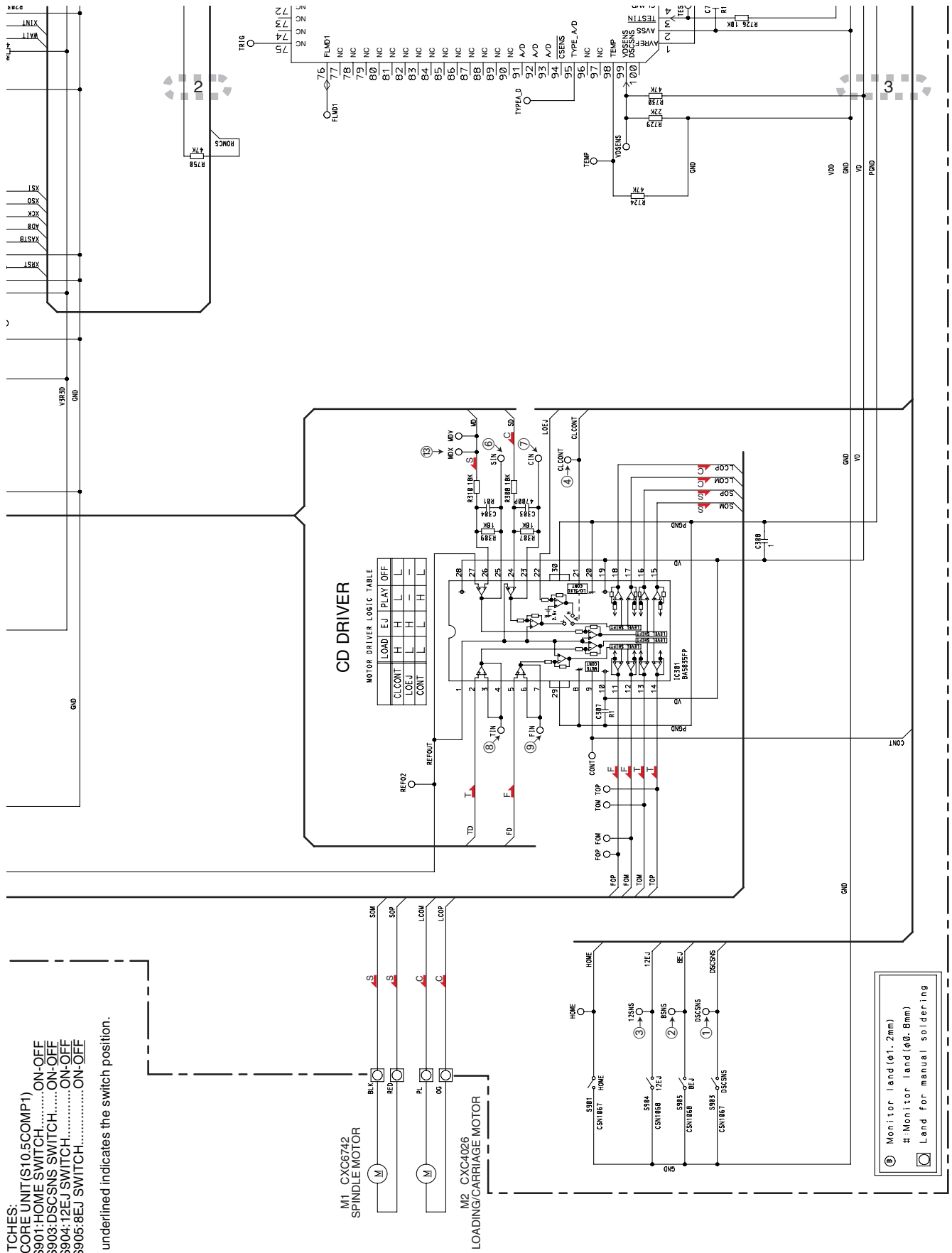


SWITCHES:  
 CD CORE UNIT(S10.5COMP1) ON-OFF  
 S901:HOME SWITCH.....ON-OFF  
 S903:DSCSNS SWITCH.....ON-OFF  
 S904:12EJ SWITCH.....ON-OFF  
 S905:8EJ SWITCH.....ON-OFF

The underlined indicates the switch position.

M1 CXG6742  
 SPINDLE MOTOR

M2 CXG4026  
 LOADING/CARRIAGE MOTOR



Ⓑ Monitor land(φ1.2mm)  
 Ⓕ Monitor land(φ0.8mm)  
 □ Land for manual soldering

C-a

NOTE1) GND ....CD LSI, RFAMP, CPU  
 PGND ...Actuator, Motor Driver  
 AGND ...Audio  
 These GND's are not connected to each other on PCB.  
 PGND is connected to a floating mechanism part by a screw.

C-a C-b

C-b







## 7.2 PARTS

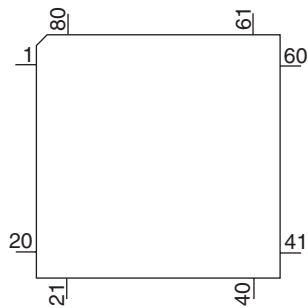
### 7.2.1 IC

#### ● Pin Functions (PE5518A)

Pin No.	Pin Name	I/O	Function and Operation
1	MODEL1	I	Model select input
2,3	NC		Not used
4	AVSS		GND
5,6	NC		Not used
7	AREF1		VDD
8	KYDT	I	Display microcomputer data input
9	DPDT	O	Display microcomputer communication data output
10	NC		Not used
11	TUNPDI	I	PLL data input
12	TUNPDO	O	PLL data output
13	TUNPCK	O	PLL clock output
14	PCL	O	Clock adjustment output
15	TESTIN	I	Test program input
16	BSI	I	Bus serial data input
17	BDATA	O	Bus serial output data
18	BSCK	O	Bus serial clock output
19	DORAON		Not used
20	NC		Not used
21	SWVDD	O	Display microcomputer chip select output
22	ILMPW	O	Illumination power output
23-31	NC		Not used
32	DALMON	O	Output for dark current reduction circuit / Stand-by mode : L output
33	VSS		GND
34	BRST	O	Bus reset output
35	BRXEN	I/O	Bus RX enable input/output
36	CDRESET	O	CD microcomputer reset signal output
37	ROMDATA	O	ROM collection data output
38	ROMCLK	O	ROM collection clock output
39	ROMCS	O	ROM collection chip select output
40	RECEIVE	O	RDS decoder receiving output
41,42	NC		Not used
43	SYSPW	O	System power output
44-46	NC		Not used
47	STRKEY2	I	Wired remote control input 2
48	MUTE	O	System mute output
49	ANTPW	O	Auto antenna control output
50	NC		Not used
51	VST	O	E.VOL strobe output
52	VDT	O	E.VOL data output
53	VCK	O	E.VOL clock output
54	NC		Not used
55	TUNPCE2	O	PLL chip enable output 2
56	TUNPCE	O	PLL chip enable output
57	RDT	I	RDS LK input
58	RDSLK	I	RDS clock input
59	RDS57K	I	RDS 57K input
60	RESET		Reset
61	LDET	I	PLL lock detection input
62	RCK	I	RDS clock input
63	ASENS	I	ACC sense input
64	BSENS	I	Back up sense input
65	DSENS	I	Grille detach sense input
66	SOURCE	I	Source sense input
67	VSS		GND
68	VDD		VDD

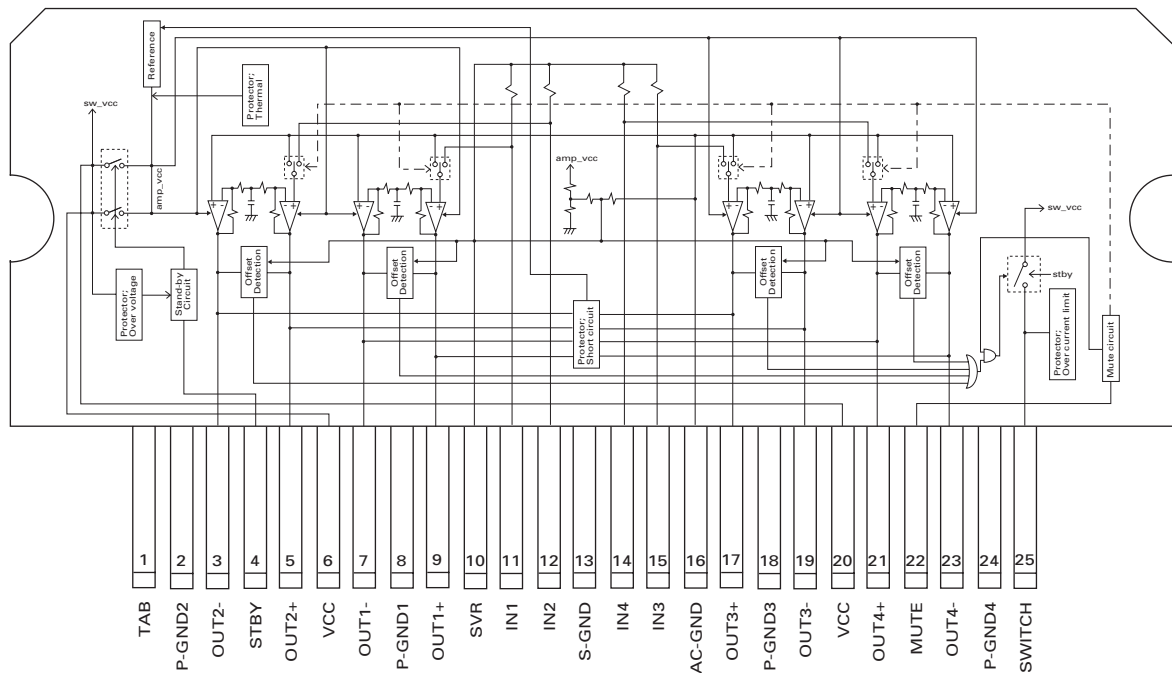
Pin No.	Pin Name	I/O	Function and Operation
69,70	X2,1		Crystal oscillator connection pin
71	IC(VPP)		GND
72	NC		Not used
73	VSS		VSS
74	AVDD		VDD
75	AVREF1		VDD
76	SL	I	Signal level input
77,78	NC		Not used
79	BSRQ	I	Bus slave service request
80	STRKEY1	I	Wired remote control input 1

\*PE5518A



IC's marked by \* are MOS type.  
Be careful in handling them because they are very liable to be damaged by electrostatic induction.

PAL007B



PML014A

● Block Diagram

● Pin Layout

A

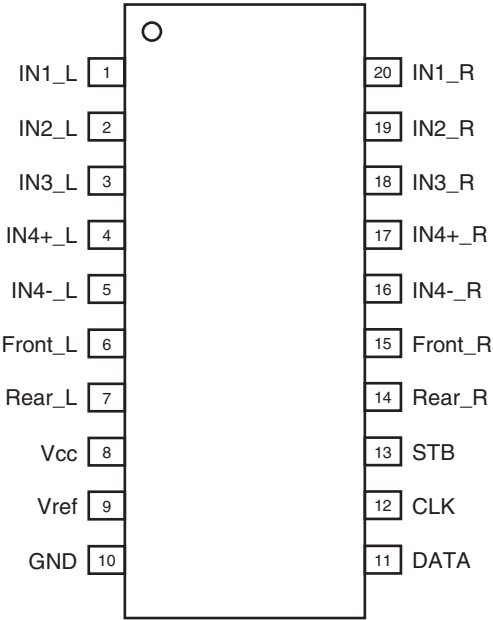
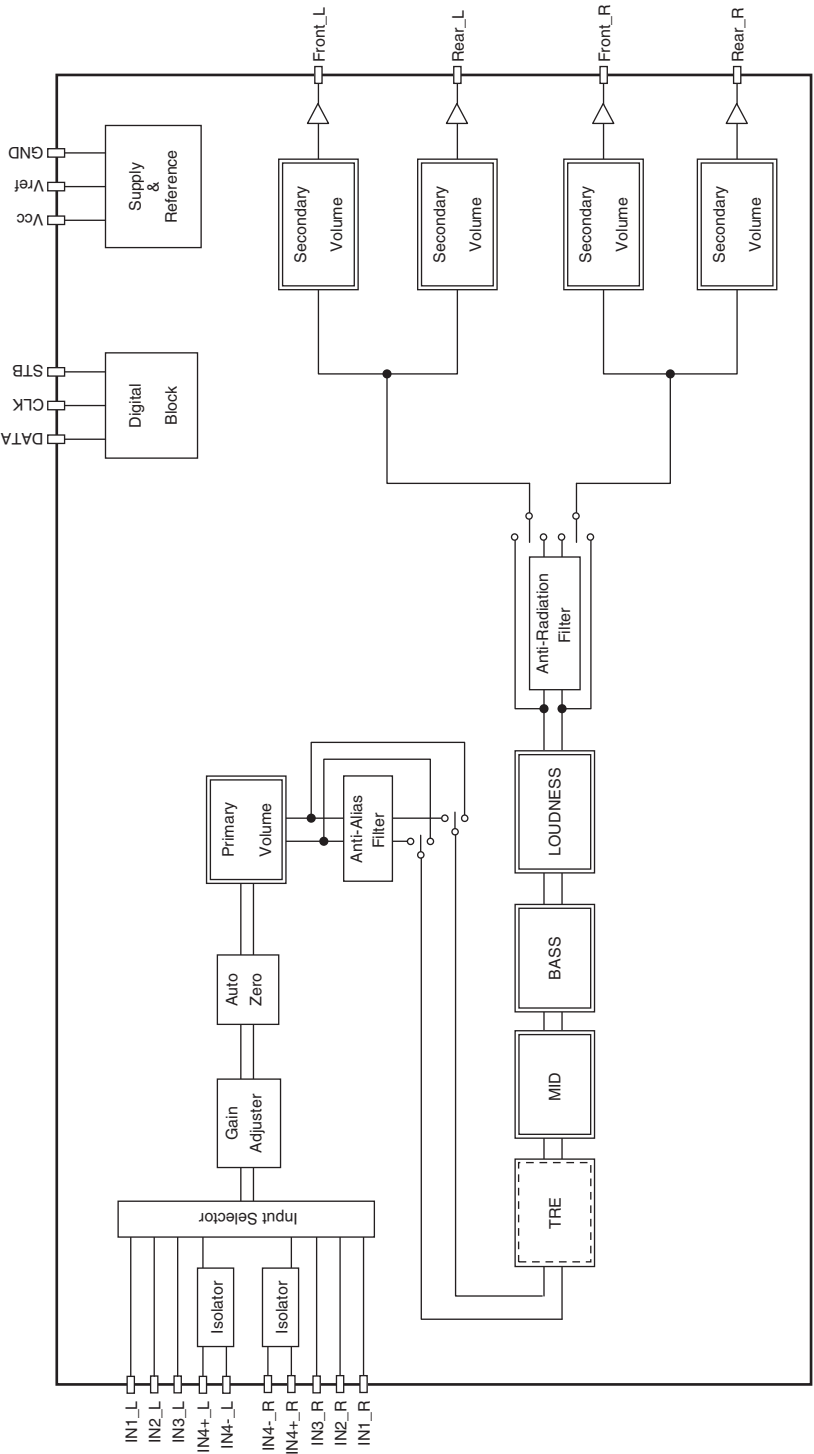
B

C

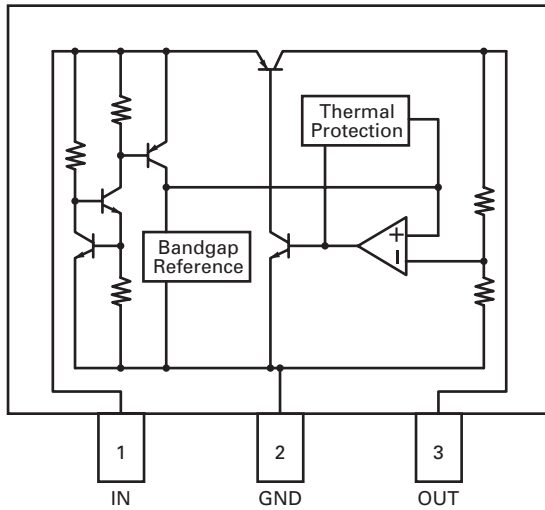
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E

F



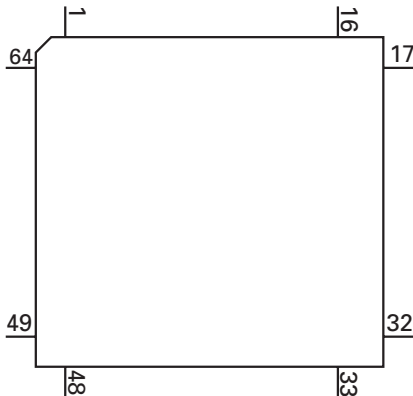
NJM2885DL1-33



### ● Pin Functions(PD6340A)

Pin No.	Pin Name	I/O	Function and Operation
1-5	SEG4-0	O	LCD segment output
6-9	COM3-0	O	LCD common output
10	VLCD		LCD drive power supply
11-14	KST3-0	O	Key strobe output
15,16	KDT0,1	I	Key data input (analogue input)
17	REW	I	Remote control reception input
18	DPDT	I	Display data input
19	NC		Not used
20	KYDT	O	Key data output
21	MODA		GND
22	X0		Crystal oscillator connection pin
23	X1		Crystal oscillator connection pin
24	VSS		GND
25,26	KDT2,3	I	Key data input
27	NC		Not used
28	KST4	O	Key strobe output
29-32	NC		Not used
33-55	SEG35-13	O	LCD segment output
56	VDD		Power supply
57-64	SEG12-5	O	LCD segment output

\* PD6340A

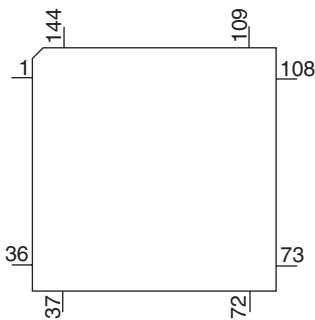


# **Pin Functions (UPD63763CGJ)**

Pin No.	Pin Name	I/O	Function and Operation
1	D.VDD		Power supply for digital circuits
2	D1.GND		Ground for 1.6 V digital circuits
3	RESET	I	Input of reset
4-8	AB12-8	I	Address bus 12-8 from the microcomputer
9-16	AD7-0	I/O	Address/data bus 7-0 to the microcomputer
17	$\overline{CS}$	I	Chip selection
18	ASTB	I	Address strobe
19	READ	I	Control signals(read)
20	WRITE	I	Control signals(write)
21	WAIT	O	Control signals(wait)
22	INTQ	O	Interruption signals to the external microcomputer
23,24	IFMODE0,1	I	Switching the microcomputer I/F 0, 1
25	D1.VDD		Power supply for 1.6 V digital circuits
26	DA.VDD		Power supply for DAC
27	ROUT	O	Output of audio for the right channel
28	DA.GND		Ground for DAC
29	REGC		Connected to the capacitor for band gap
30	DA.GND		Ground for DAC
31	LOUT	O	Output of audio for the left channel
32	DA.VDD		Power supply for DAC
33	X.VDD		Power supply for the crystal oscillator
34	XTAL	I	Connected to the crystal oscillator(16.9344 MHz)
35	XTAL	O	Connected to the crystal oscillator(16.9344 MHz)
36	X.GND		Ground for the crystal oscillator
37	VDDREG15		Control of 1.6 V regulator
38	PWMSW0	I	Setup 0 for PWM output(SD, MD)
39-41	TEST3-1	I	Connected to Ground
42	PWMSW1	I	Setup 1 for PWM output(FD, TD)
43	TESTEN	I	Connected to Ground
44	D1.GND		Ground for 1.6 V digital circuits
45	DIN	I	Input of audio data
46	DOUT	O	Output of audio data
47	SCKIN	I	Clock input for audio data
48	SCKO	O	Clock output for audio data
49	LRCKIN	I	Input of LRCK for audio data
50	LRCK	O	Output LRCK for audio data
51	$\overline{XTALEN}$	I	Permission to oscillate 16.9344 MHz
52	D1.VDD		Power supply for 1.6 V digital circuits
53	RFCK/HOLD	O	Output of RFCK/HOLD signal
54	WFCK/MIRR	O	Output of WFCK/MIRR signal
55	PLCK/RFOK	O	Output of PLCK/Output of RFOK
56	LOCK/RFOK	O	Output of LRCK/Output of RFOK
57	C1D1/C8M/(RA13)	O	Information on error correction/C8M : 8 MHz
58	C1D2/C16M/(RA12)	O	Information on error correction/C16M : 16 MHz
59	C2D1/RMUTE	O	Information on error correction/Mute for Rch
60	C2D2/LMUTE	O	Information on error correction/Mute for Lch
61	C2D3/SHOCK	O	Information on error correction/Detection of vibration
62	D1.GND		Ground for 1.6 V digital circuits
63	C33M	O	Output of 33.8688 MHz(CLK for SDRAM)
64	(RCS)	O	DRAM $\overline{CS}$
65	RA11	O	Output of DRAM address 11
66	(CKE)	O	Output of DRAM CKE
67	RAS	O	Output of DRAM RAS
68	$\overline{CAS0}$ (LDQM)	O	Output of DRAM lower $\overline{CAS}$ (LDQM)
69	$\overline{CAS1}$ (UDQM)	O	Output of DRAM upper $\overline{CAS}$ (UDQM)

Pin No.	Pin Name	I/O	Function and Operation
70	WE	O	Output of DRAM WE
71	OE(CAS)	O	Output of DRAM OE(CAS)
72	D.GND		Ground for digital circuits
73-88	RDB0-15	I/O	Input/output of DRAM data0-15
89-99	RA0-10	O	Output of DRAM address0-10
100	D.VDD		Power supply for digital circuits
101	FD+	O	Output of focus drive PWM +
102	FD-	O	Output of focus drive PWM -
103	TD+	O	Output of tracking drive PWM +
104	TD-	O	Output of tracking drive PWM -
105	SD+	O	Output of thread drive PWM +
106	SD-	O	Output of thread drive PWM -
107	MD+	O	Output of spindle drive PWM +
108	MD-	O	Output of spindle drive PWM -
109	REFOUTSV	O	REFOUT for servo
110	AD.VDD		Power supply for ADC
111	EFM	O	Output of EFM signals
112	ASY	I	Input of asymmetry
113	ATEST	O	Analog tests
114	RFI	I	Input of RF
115	AD.GND		Ground for the analog system
116	AGCO	O	Output of RF
117	C3T	O	Connection to the capacitor for detecting 3T
118	AGCI	I	Input of AGC
119	RFO	O	Output of RF(AGC)
120,121	EQ2,1	I	Equalizer 2, 1
122	RF2-	I	Reversal input of RF2
123	RF-	I	Reversal input of RF
124	A.GND		Ground for the analog system
125	A	I	Input of A
126	C	I	Input of C
127	B	I	Input of B
128	D	I	Input of D
129	F	I	Input of F
130	E	I	Input of E
131	VREFIN	I	Input of reference voltage
132	A.VDD		Power supply for the analog system
133	REFOUT	O	Output of reference voltage
134	REFC	I	Connected to the capacitor for output of REFOUT
135	FE-	I	Reversal input of FE
136	FEO	O	Output of FE
137	ADIN	I	Input of FE, TE A/D converter
138	TE-	I	Reversal input of TE
139	TEO	O	Output of TE
140	TE2	O	TE2
141	TEC	I	TEC
142	LD	O	Output of LD
143	PD	I	Input of PD
144	D.GND		Ground for digital circuits

\* UPD63763CGJ



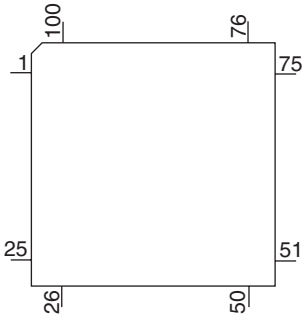
# **Pin Functions (PE5505A)**

Pin No.	Pin Name	I/O	Format	Function and Operation
1	AVREF			A power supply / Positive power supply(5V)
2	AVSS			A power supply GND
3	TESTIN	I		Chip check test program starting input
4	CLAMP			Not used
5	EVDD			E power supply / Positive power supply
6	FMODE			For flash rewriting / L : flash rewriting mode
7	FLRQ			For flash rewriting / Reset voltage control
8	IC/FLMOD0			IC : VSS direct connection/FLMOD0 : Pull-down
9	VDD			Positive power supply(5V)
10	REGC			Connected to the capacity stabilizing output of the regulator
11	VSS			GND
12	X1	I		Oscillator connection for mainclock
13	X2			Oscillator connection for mainclock
14	RESET	I		System reset input
15	XT1	I		Connected to the oscillator for subclock(connected to VSS via the resistor)
16	XT2			Connected to the oscillator for subclock(Open)
17	PULLDOWN	I		Connected to EVDD or EVSS via the resistor
18	EJSW			Not used
19	XINT	I	C	CD LSI interruption signal input
20	NC			Not used
21	BRST	I		Bus reset input
22	BSI	I		Bus serial data input
23	BSO	O	C	Bus serial data output
24	BSCK	I/O	/C	Bus serial clock input/output
25	FTxD	O	C	For flash rewriting(transmitted signal)
26	FRxD	I		For flash rewriting(received signal)
27	BRXEN	I/O	/C	Bus RX enable input/output
28	BSRQ	I/O	/C	Bus serial clock input/output
29	DSPOK			Not used
30	DSCSNS	I	C	Disc state sense input
31	8EJ(S905)	I	C	input of detection of 8 cm disc ejection
32	12EJ(S904)	I	C	input of detection of 12 cm disc ejection
33	EVSS			E power supply GND
34	EVDD			E power supply / Positive power supply
35,36	SRAMLEVEL0,1	O		SRAM level meter output
37	EMPH	O	C	Emphasis information output
38	EMPH			Not used
39	CDMUTE			Not used
40	LOEJ			Not used
41	CLCONT	O		Driver input switching output
42	HOME	I		Home SW sense input
43	ADENA	O	C	A/D reference voltage supply control output
44	LRCKOK	O	C	(DOUT mute output)
45	SRAMLEVEL2	O	C	SRAM level meter output
46	CD3VON(MCKRQ)	O	C	CD + 3.3 V power supply control output(Digital output : MCKRQ)
47	CONT	O	C	Servo driver power supply control output
48	XRST	O	C	CD LSI reset control output
49	VDCONT	O	C	VD power supply control output
50	XSI	I		CD LSI serial data input
51	XSO	O	C	CD LSI serial data output
52	XCK	O	C	CD LSI serial clock output
53	XWAIT	I	C	CD LSI wait control signal input
54	XASTB	O	C	CD LSI address strobe output
55	AD0	O	C	Address/data Bus 0
56	INT			Not used



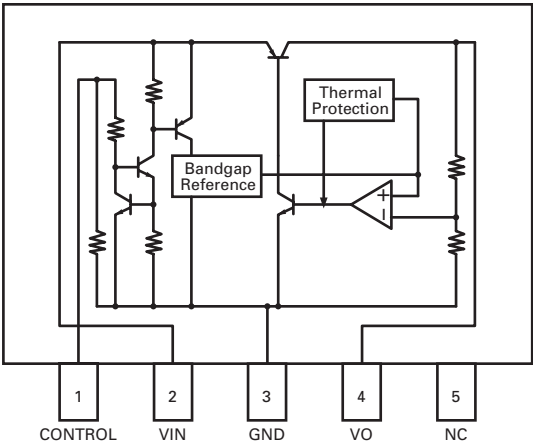
Pin No.	Pin Name	I/O	Format	Function and Operation
57	ROMDATA	I/O		E2PROM data input/output
58	ROMCK	O		E2PROM clock output
59	ROMCS	O	C	E2PROM chip selection output
60,61	NC			Not used
62	CLKOUT			Not used
63	LOCK	I		Spindle lock input
64-68	NC			Not used
69	BVSS			B power supply GND
70	BVDD			B power supply / Positive power supply
71-75	NC			Not used
76	FLMD1	I/O	/C	Address/Data Bus 5
77-90	NC			Not used
91-93	A/D			Not used
94	CSENS			Not used
95	TYPE_A/D			Not used
96,97	NC			Not used
98	TEMP			Not used
99	VDSNS	I		VD power supply short sense input
100	DSCSNS			Not used

\* PE5505A

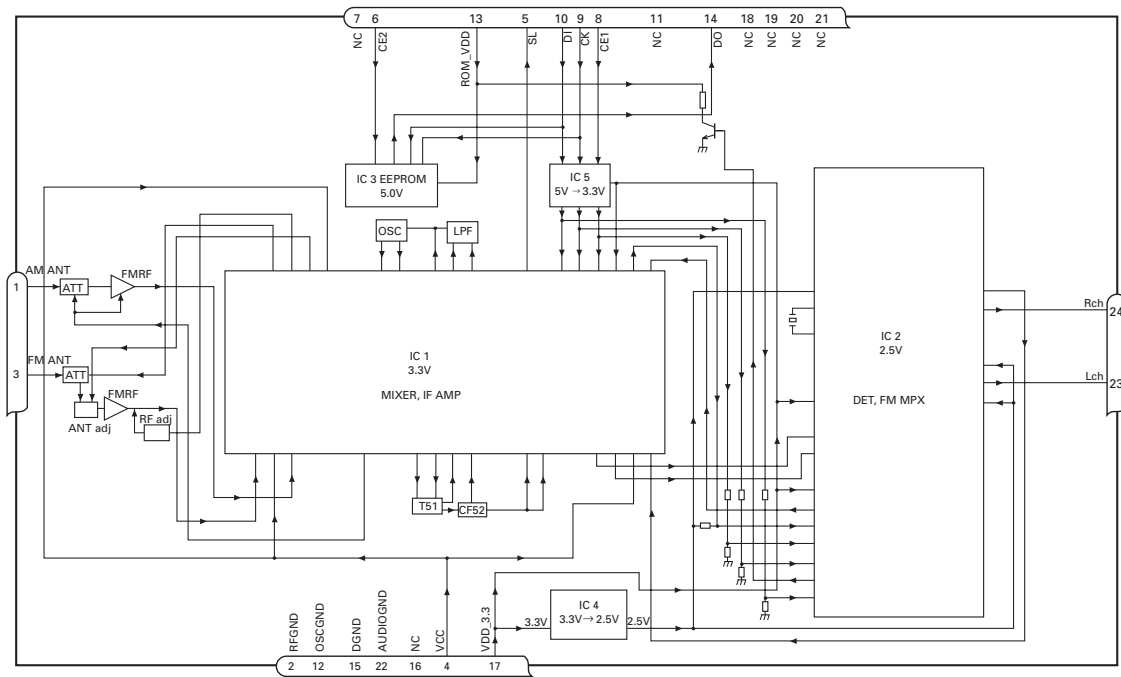


Format	meaning
C	C MOS

NJM2886DL3-33



# FM/AM Tuner Unit



No.	Symbol	I/O	Explain
1	AMANT	I	AM antenna input AM antenna input high impedance AMANT pin is connected with an all antenna by way of 4.7μH. (LAU type inductor) A series circuit including an inductor and a resistor is connected with RF ground for the countermeasure against the hum of power transmission line.
2	RFGND		RF ground Ground of antenna block
3	FMANT	I	FM antenna input Input of FM antenna 75Ω Surge absorber(DSP-201M-S00B) is necessary.
4	VCC		power supply The power supply for analog block. D.C 8.4V ± 0.3V
5	SL	O	signal level Output of FM/AM signals level
6	CE2	I	chip enable-2 Chip enable for EEPROM "Low" active
7	NC		non connection Not used
8	CE1	I	chip enable-1 Chip enable for AF•RF "High" active
9	CK	I	clock Clock
10	DI	I	data in Data input
11	NC		non connection Not used
12	OSCGND		osc ground Ground of oscillator block
13	ROM_VDD		power supply Power supply for EEPROM pin 13 is connected with a power supply of micro computer.
14	DO	O	data out Data output
15	DGND		digital ground Ground of digital block
16	NC		non connection Not used
17	VDD_3.3		power supply The power supply for digital block. 3.3V ± 0.2V
18	NC		non connection Not used
19	NC		non connection Not used
20	NC		non connection Not used
21	NC		non connection Not used
22	AUDIOGND		audio ground Ground of audio block
23	L ch	O	L channel output FM stereo "L-ch" signal output or AM audio output
24	R ch	O	R channel output FM stereo "R-ch" signal output or AM audio output